# KEYPOINT
# IN AUTOMATION

## Company Profile

ines-Innovative Elektronik Systems was founded in 1985 by Friedel Hacker and Wolfgang Schilling. The first product developed by ines was an IEEE488 interface system for MS-, PC- and DR-DOS. The product range has since been expanded considerably and now counts various IEEE488 boards for different computer bus systems (ISA/EISA, PS/2 MicroChannel, Toshiba EXT, AT-96, ISA-96, PCMCIA, PCI, Compact PCI) with driver software for the most established operating systems in test & measurement, such as MS-, PC-, DR-DOS and MS-Windows, MS-Windows NT, OS/2 and UNIX SCO, 386/ix Interactive, AIX, XENIX, Solaris, SICL (HP) etc.

Over the last years ines has continuously advanced and expanded the company's export business. Documentations in English and French eased the way to enter foreign markets. Today ines is represented by distributors and OEMs in all European countries as well as in the USA, Canada, Israel, Korea, Singapore, Hongkong, Taiwan and Japan.

The high standard in technology together with various quality controls allow ines to grant a five year warranty on the IEEE488 hardware. The so-called 'non-option-policy' includes services such as free driver updates.

These updates allow the user to work with the latest programming languages without any extra costs for extended driver functions.

A support-hotline is the interface to the ines development department and offers a most efficient support for the ines products. Any user of an original ines product is entitled to make use of the support service which is provided either by fax, phone or by e-mail.

Functionality of the ines product lines is continuously extended and improved in order to respond to the demand in the market and suit the customer. Modifications regarding the hardware are always in correspondence with the principle of backward and forward compatibility. Most recently ines presented the company's new strategic developments: the IEEE488.2 controller chip series, the IEEE488.2-PCMCIA card, the Real Time VICENT VXIbus controller, and ISCRIPT, an object oriented CLIENT-SERVER software for complex applications under OS/2, MS-Windows NT and UNIX. The new product lines very well reflect the technological know-how of ines in the whole area of test & measurement and automation.

## The ines GPIB CHIP

### The IEEE488 Standard

In 1965 Hewlett-Packard developed the HP-IB (Hewlett Packard Interface Bus), a bit parallel and byte serial 8-bit communication and control interface with a 3 line handshake (DAV, NRFD, NDAC) for a maximum of 15 devices on the bus and a theoretical transfer rate of 1 Mbytes/s. The HP-IB was registered in 1975 by the IEEE (Institute of Electrical and Electronic Engineers) as IEEE488 standard and also gained international importance under GPIB (General Purpose Interface Bus).

In the 90s the market for the IEEE488 bus exponentially increased together with the booming PC market. In 1987 the IEEE extended the standard to IEEE488.2. Over the last couple of years the GPIB market developed significantly. The extension of the IEEE488.2 including SCPI bears various advantages for the user. IEEE488.1 is the basis of the IEEE488.2

standard and deals with the mechanical and electrical issues and the transmission protocols.

IEEE488.2 is an extension regarding to exact timing definitions, instrument syntax and common commands - generally known as IEEE488 commands. This means that software commands and instruments may now easily be exchanged, and existing application software may still be used without any problems. The instrument command sets have been unified under SCPI saving the user now time and programming efforts.

Especially with the recent efforts in IEEE488.2 chip development and advanced and faster computer and instrument technologies the IEEE488.2 standard has a very prosperous future outlook. Even though challenged by other standards, such as the VXIbus, the IEEE488.2 standard has proved to be a mature and highly efficient standard for years. The standard definitions are continuously updated according to latest developments in test & measurement and asure an up-to-date performance, that will not be replaced easily by any future developments.

## iGPIB Controller Chip

The development of the iGPIB controller chip according to the IEEE 488.2 standard was technologically inevitable for ines. Besides software compatibility with the popular NEC 7210c and TMS 9914A, the 40 pin DIP chip and the 44 pin PLCC will also be pin compatible. The chip architecture was designed by ines and technologically realized by IAD.

The different packagings of the chip will in the following mainly be distinguished by either referring to DIP (40 pin Dual Inline Packaging) or PLCC and QFP (44 and 80 pin for SMD). A list of the currently available chips and those available in November 98 has been included.

As a strategic development the iGPIB had to meet various requirements. The chip had to be software and pin compatible with the NEC 7210c and/or TMS 9914A and meet all requirements and optional recommendations of the IEEE 488.2 standard definitions, and should have all new features specified by ines. The development tool for the Full Custom Design chip was a „SaganTec“ silicon compiler. The power and flexibility of this tool lead to the decision to develop an 8-bit DIP chip and a PLCC chip that supports computer busses of up to 128 bit. In order to avoid all known disadvantages of the asynchronous design the iGPIB was developed as an entirely synchronous design. All iGPIB packaging designs (DIP, PLCC and QFP) are available as NEC 7210c or TMS 9914A software compatible versions. In addition the 40 pin DIP design is pin compatible and may replace the NEC 7210c or TMS 9914A in instruments and on controller boards. Regarding the Texas Instruments compatibility there will also be a 44-pin PLCC design available. Nevertheless, the 44-pin PLCC is available with the NEC 7210 compatibility as well on request. ines herself uses the 40 pin DIP NEC 7210 compatible chip on the 8-bit ines boards. The 16-bit boards are accordingly equipped with the 80 pin chip in the second generation.

Besides the NEC 7210c & TMS 9914A compatibility all compulsory and optional features of the IEEE488.2 standard are supported, such as the Find Listener Protocol. In addition special ines features have been implemented. The 68-pin iGPIB was strategically designed to become an important part of the new VICENT VXIbus Controller Family of ines and the 80-pin QFP for the new PCMCIA cards.

The 40 pin DIP is a fast 8-bit chip. It may be used as controller chip and in instruments as device chip. One of the significant features is the transfer rate of 1,3 MByte/s under software control and 30 MByte/s in synchronous DMA mode. The DMA-STATE-MACHINE, known from the ines/AT/boards, has been implemented in the iGPIB. All packaging designs have integrated 2x255 Byte FIFOs. The technical details are described in the according chapters.

The >68 pin chips are equipped with two FIFO buffers, the DMA-STATE-MACHINE and support up to 128 bit busses. It reaches transfer rates of 2,5 (max. up to 4) MByte/s under software control and a maximum rate of 30

MByte/s in the FIFO buffer memory transfer when writing into the FIFO.

All iGPIBs will also be available as device chips (Talker/Listener) for instruments. Technical features as well as transfer rates are identical with the controller chip versions. The iGPIB device chips are offered including ines-ieee488.2 device driver software, which is described later on.

An extended command set reduces the software overhead, which was, for example, not possible in NEC 7210c applications. The iGPIB chip is fully IEEE488.2 compatible. At the same time bus control and bus monitoring have been improved. The iGPIB has i.e. integrated timer and data byte counter. A Last Byte Handling feature may automatically generate a Handshake Holdoff on read operations, or EOI on write operations. This function is of high advantage working under Multi-user/Multi-Tasking operating systems, because device drivers need less interrupts and so operate much faster.

The new ines-ieee488.2 boards with the ieee-488.2 driver software represent a new generation of innovative automation systems. Existing NEC 7210c and TMS 9914A applications can easily be integrated with the iGPIB in order to allow the use of existing drivers.

Currently ines offers the DIP and PLCC iGPIBs as a controller chip and/or as a device chip (Talker/Listener). For new developments ines recommends the 72010 iGPIB with integrated IEEE488 bus drivers (SN 75160 & SN 75162). Existing instruments equipped with the NEC 7210c or TMS 9914A may easily be upgraded to IEEE488.2 by simply installing the NEC or TMS pin compatible 40-pin DIP or 44-pin PLCC iGPIB. The according ines-ieee488.2 device-driver is EPROM capable and makes it easy to upgrade existing IEEE488.1 instruments to the IEEE488.2 standard with SCPI. However, the 68/80 pin PLCC chips provide additional advantages regarding transfer rates. The 80 pin version also have integrated ISA interface and IEEE488 bus drivers.

## Functional Characteristics of the iGPIB

The iGPIB performs various functions in order to provide a high-performance microprocessor interface to the GPIB. ATE system performance is accelerated remarkably.

## NEC 7210c & TMS 9914A Compatibility

RESET changes the original iGPIB (= native mode) mode into the NEC 7210c or TMS 9914A compatible mode (M7210 or M9914). This mode is enabled until the iGPIB is switched to native mode (M4882) using the M4882 auxiliary command. The M7210 or M9914 mode guarantees NEC 7210c or TMS 9914A software compatiblility for all existing NEC 7210c or TMS 9914A applications.

In order to exploit all additional IEEE488.2 functions and the special ines features the M4882 native mode is recommended for new developments allowing the use of all iGPIB features.

The iGPIB represents a software and/or pin compatible replacement for the NEC 7210c or TMS 9914A provided that a 30 MHz Clock Source is used (the NEC 7210c uses 1...8 MHz / the TMS 9914A uses a 0,5...5 MHz clock). The new iGPIB generation which will be launched in November 98 will use an 8 MHz Clock Source as replacement for the NEC 7210c and a 4 MHz Clock Source as replacement for the TMS 9914A. No changes have to be made by the user.

## Data Transfer

The data transfer to or from the GPIB is performed via two 255 Byte wide FIFO registers/buffers. These FIFOs are used to decouple GPIB data traffic from the CPU bus.

Using the iGPIB as an IEEE488.2 device, the FIFOs may be used as the input or output queue what simplifies the software design significantly. In addition, provisions were made to support the IEEE488.2 Trigger Control and to support the MAV (Message Available) Reset

directly in the hardware. The last feature is unique by ines.

The FIFOs may be accessed respectively with simple „read“ and „write“ operations (to the DIR or CDOR). Using this technique combined with repetitive move instructions (i.e. REP INSB of the 80386 CPU) allows to use the full 1 MByte/s band width without using DMA.

## Timeout

The iGPIB provides a timeout interrupt condition. If the condition is unmasked, a timer counts down for a programmable interval. Any time a data transmission takes place, the timer will be reset to its original (programmed) value. If the handshake gets stuck, the timer underflows and an interrupt occurs. The timeout is from 1 ms up to 65 s in resolution of 1 ms. Normally the timeout functionality had to be provided by the interface driver software, which is not necessary anymore now

## Transfer Counter

The iGPIB offers a 16-bit wide transfer counter. This counter reduces the programming for DMA operations in two ways.

First, the counter delivers an end-of-transfer interrupt, if a programmable amount of data has been sent or received, respectively. The driver software can initiate a DMA transfer and then switch to another task until the interrupt occurs.

Second, a Last Byte Handling feature allows to automatically send the last byte with EOI true. This means, on send transfers (talker), it indicates the end of a data block. On receive transfers, it is possible to automatically signal NRFD active after the last byte has been received (listener). With previous GPIB controllers, like the NEC 7210c, all these operations had to be programmed explicitly via software.

## IEEE488.2 Service Request

In order to integrate the preferred IEEE488.2 implementation of requesting service, the iGPIB realizes the Service-Request-Enable register on chip. This allows to update the status byte via the status byte register independent of requesting service. Together with two transition filters for each status bit, the iGPIB handles the service request generation autonomously without any software intervention. Further, the MAV bit of the IEEE488.2 status byte can be reset automatically, if a message (data block) has been sent. This solves the problem of differing speeds between device and controller, which has not been specified sufficiently in the IEEE488.2 standard.

## Stop-Handshake Condition

The IEEE488.2 standard explicitly recommends more than one stop-handshake condition for an IEEE488.2 Controller. Previous Controllers allow only to use EOI and one EOS byte. The iGPIB instead allows to use EOI and up to three EOS bytes. The iGPIB entirely meets the IEEE488.2 standard recommendations in hardware, at the same time reducing the software overhead. In addition, the Controller allows to ignore EOI as a stop-handshake condition. This simplifies the handling of pre-488.2 devices and devices not entirely operating according to the standard.

## Bus Line Control and Monitoring

The iGPIB independently controls and monitors each bus line as well as the transceiver control signals. This feature exceeds the IEEE488.2 requirements (monitoring NRFD and NDAC).

## Synchronous DMA Interface

The iGPIB FIFOs may be accessed via the synchronous DMA interface (XDMA). This interface enables FIFO access without using the CPU data bus. XDMA can transfer data at a speed of up to 30 MByte/s. This interface may be used for various purposes. High speed / high perfomance instruments, for example, may transfer data directly to the GPIB FIFO without any CPU intervention. Computers acting as

GPIB controllers can perform DMA cycles utilizing the full band width of their busses, i.e. even with 64-bit architectures, up to 128 bit busses.

## ines-ieee488.2 Device Driver Software

For instrument manufacturers ines decided to ease the upgrading of the IEEE488.1 to 488.2 standard definitions with SCPI by offering the ines-ieee488.2 device driver software in a package together with the developer kit of the chip. The licence for the driver is free of charge and provides the user with the latest features of the IEEE488.2.

This software provides routines to the iGPIB chip in IEEE488.2 devices. It may also be used for systems which do not use the IEEE488.2 protocol, but require a GPIB stream-like interface.

The software is written in ANSI compatible C and may be compiled for any microprocessor.

The iGPIB developer kit includes the ines-ieee488.2 device driver software (for instruments only). This software may be adapted to any hardware platform easily. For demonstration reasons ines provides a demo package for PC's. The demo shows how to use the device driver software and reduces any programming effort for the engineer. In the future ines will also provide adaptions for popular SCPI interfaces.

All iGPIB designs as described above support the requirements and optional recommendations of the IEEE488.2 standard and are backwards compatible to existing NEC 7210c or TMS 9914A applications. They are offered as controller chip or device chip (Talker/Listener). For the device chip versions ines offers an IEEE488.2 device driver software. Instrument manufacturers presently using the NEC 7210c or TMS 9914A can easily upgrade IEEE488.1 instruments by simply replacing it with the according iGPIB.

In addition, the FULL CUSTOM DESIGN allows to integrate mircorprocessors as MACRO including BASIC PROM, or even A/D & D/A circuits as well as customer specific circuits. The 80 pin iGPIBs 80 have integrated IEEE drivers (SN 75160 + SN 75162). The 80 pin iGPIB has the full functionality of the ines 16-bit AT board or an PCMCIA interface integrated. Naturally, all iGPIBs are equipped with the two 255 byte FIFOs.

## Summary

In summary one can say that the development of the iGPIB represents a significant step into the future of GPIB measurement systems. The intention of ines was to launch a chip, whose technical design, complexity and performance are the guarantee for an investment into the future.

For more detailed information about the iGPIB controller chip see the iGPIB Hardware Manual.

| Features | Type | | | | | |
|---|---|---|---|---|---|---|
| | i7210 | i9914 | i72010 | i-D-72010 | i-ISA-72010 | i-PC-72010 |
| Full Custom Design | YES | YES | YES | YES | YES | YES |
| Packaging Type | 40 DIP | 40 DIP<br>44 PLCC | 68 PLCC | 80 QFP | 80 QFP | 80 QFP |
| NEC 7210c pin compatible | YES | - | - | - | - | - |
| TMS 9914 pin compatible | - | YES | - | - | - | - |
| Software compatible with NEC 7210 and TMS 9914 | YES | YES | YES | YES | YES | YES |
| Settling time T1 min. | 250ns | 250ns | 250ns | 250ns | 250ns | 250ns |
| FIFO buffer in byte | 2x255 | 2x255 | 2x255 | 2x255 | 2x255 | 2x255 |
| Transfer rate AT-bus under software control per sec. | 1.2MB | 1.2MB | 2.5MB | 2.5MB | 2.5MB | 2.5MB |
| Max transfer rate FIFO->computer bus | 30MB | 30MB | 30MB | 30MB | 30MB | 30MB |
| Supported computer bus width in bit | 8 | 8 | 128 | 128 | AT bus | PCMCIA bus |
| 16 bit ISA interface | - | - | - | - | YES | - |
| 16 bit PCMCIA interface | - | - | - | - | - | YES |
| IEEE-488 transceiver integrated (SN75160 + SN75162) | YES* | YES* | YES* | YES | YES | YES |
| Available as IEEE-488.2 controller and device chip | YES | YES | YES | YES | YES | YES |
| Automatic terminator recognition | YES | YES | YES | YES | YES | YES |
| Max. of recognized EOS bytes | 3 | 3 | 3 | 3 | 3 | 3 |
| Automatic handshake holdoff | YES | YES | YES | YES | YES | YES |
| Automatic transfer of complex SCPI strings | YES | YES | YES | YES | YES | YES |
| Automatic MAV reset | YES | YES | YES | YES | YES | YES |
| T8 timer support (IFC time) | YES | YES | YES | YES | YES | YES |
| Hardware trigger disable (necessary for IEEE-488.2) | YES | YES | YES | YES | YES | YES |
| Device driver software (no charge for licence) | YES | YES | YES | YES | YES | YES |
| Available as software macro for integrated custom designs | YES | YES | YES | YES | YES | YES |
| Sleep mode | - | - | - | YES | YES | YES |
| Clock source | 8/30MHz* | 4MHz* | 30MHz | 30MHz | 30MHz | 30MHz |
| Low Power 3.3 V | - | - | - | YES | YES | YES |

Options:
Integrated Fiber Optic Controller
Integrated processors like 8051 with basic PROM

* Available November 98
** 30 MHz actual used, new generation (available November 98) uses 8 MHz