DAQ i218
Hardware Manual

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1. OVERVIEW

Before using the DAQ i218, take some time to read the section **"OPERATIONAL PRECAUTIONS".**

The DAQ i218 card is a general purpose Analogue Data Acquisition card with the following features:

- 21-bit sampling AtoD converter
- 8 differential or 16 single ended analogue inputs
- 8 digital I/O lines
- On card temperature sensor
- Accurate voltage reference
- Full CIS in EPROM
- 10MHz oscillator
- Programmable clock divider
- Snap shot input mode with interrupt
- Fault protection on analogue lines
- Programmable pull up-or-down on all 8 digital lines
- Programmable open-drain mode on all 8 digital lines

This guide aims to familiarise you with the way that the DAQ i218 works and so will help you to maximise its performance in your application.

2. ABOUT THE DAQ i218

The DAQ i218 uses a ΣΔ (sigma-delta) A to D converter chip. It is made by Analogue Devices and its part number is AD7710. You are strongly advised to obtain a data sheet for this device to fully understand the workings of the chip. The following section will provide a quick discussion of the AD7710's operation.

2.1 QUICK THEORY OF ΣΔ CONVERTERS

This type of converter uses a "charge balancing" technique to approximate the analogue level being applied to its input. A capacitor internal to the AD7710, holds the difference between the actual input and the approximated input (i.e. the output). A control loop in the converter attempts to maintain this difference at zero. The "effort" the ΣΔ circuit applies in increasing or decreasing the capacitor charge (in order to track the input voltage) is reflected inside the converter as the duty cycle of the output of the control circuit that is making an "above-or-below" decision. To achieve a high number of effective bits of resolution, the AD7710 "looks" at the input voltage at a rate of at least 20KHz (the actual rate depends on the gain programmed in the AD7710's control register). This means that the "noise" produced in the output data that comes from making a simple "above-or-below" decision is spread across a much wider bandwidth than the one of interest (this is called oversampling). The "above-or-below" decision is made by a comparator which in turn controls a 1-BIT DtoA converter (a 1-BIT DAC has only two output states: +Vmax and -Vmax). It is this DAC that generates the voltage that is summed with the input voltage in an attempt to zero out the capacitor charge. This is why ΣΔ converters all sometimes called 1-BIT oversampling converters.

The net result of oversampling the input with a 1-BIT resolution, is that by digitally filtering the duty cycle data emerging from the control loop a much higher "effective resolution" can be realised across a smaller bandwidth. So oversampling the input at 20KHz the AD7710 can end up with an ENOB (effective number of bits) of over 20 when the digital filter is programmed to filter down the

output data to a bandwidth of 3Hz (10Hz output data rate). Here, the oversampling ratio is 20KHz/10Hz or 2000:1.

The AD7710 is optimized to generate high ENOBs with very low output data rates (i.e. a few tens of hertz). The output data rate should not be confused with the sampling rate at the input of the AD7710. At higher data rates the AD7710 is not so good.

The other aspect of the AD7710 which must be remembered is that the internal digital filter cannot react to step inputs very quickly. At worst (4 x DATA UPDATE RATE) seconds should be allowed for it to settle. At a 10Hz output rate this means 4 x 100ms. This step could be a "spike" in the input voltage or could be caused by switching input channels on the DAQ i218.

2.2 NOISE

Noise is the main cause of degradation in the ENOB rating of the ΣΔ converter. The noise from the converter itself (thermal, quantisation etc.) are all taken into account in the tables of Effective Resolution for the AD7710 (see Specification section).

The ENOB of a converter is expressed as:

ENOB = (SNR(dB) - 1.76) / 6.02

So, the better the signal to noise ratio the higher the effective resolution. Be warned however, that this computation is based on RMS noise. Taking individual samples from the AD7710 will reveal that the noise is Gaussian in distribution and is subject to the usual statistical spread in its peaks and troughs from moment to moment. So the converter output looks noisy, or at least more noisy than you might expect. *To achieve the stated ENOB, some kind of post-processing of the data samples will be required in software*. This may mean a simple averaging process over say 10 or more samples, or could be a properly designed digital filter. This will depend on the exact application. Bear in mind that this averaging could further reduce the bandwidth of the data you are acquiring and will increase the settling time needed for step-input changes.

The DAQ i218 inevitably introduces several extra sources of noise:

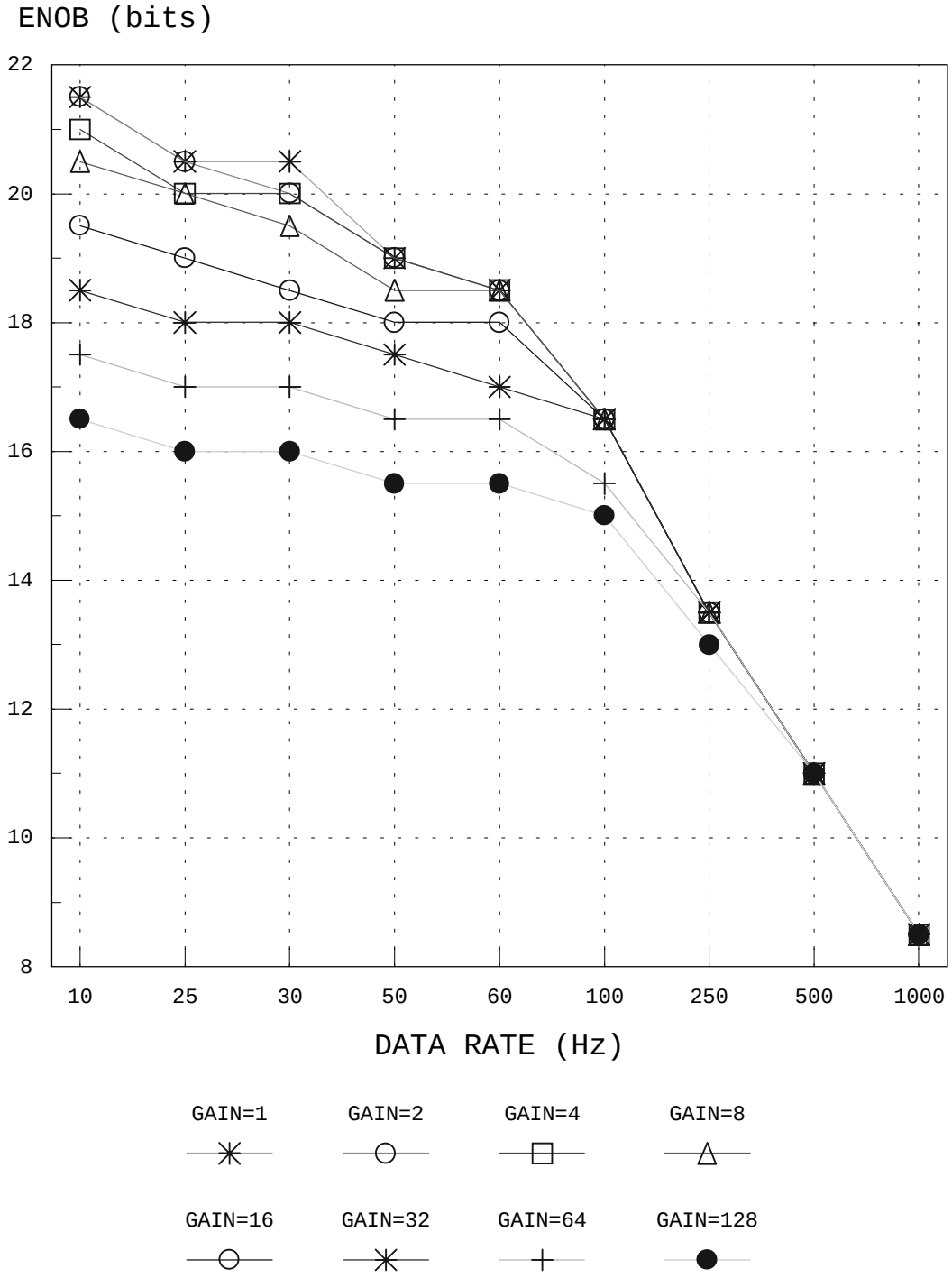
- The voltage reference (an AD680J)
- The power rails (largely noise from the PC's supplies)
- Ground noise
- Noise from the front-end analogue multiplexers. This will be noise injected from the power rails + thermal noise in mosfet channels + charge packets injected into the analogue path when the multiplexer channel is switched.

All of these noise sources will act to degrade the ENOB attainable with the DAQ i218. As a very rough guide, with a gain of 1, bipolar mode, 10Hz output data rate, single ended inputs ranging from +2.5V to -2.4V referenced to AGND, a single conversion data word will have around 20μV of pk-pk noise riding on it. Put another way, if you were to watch the samples from the DAQ I218 coming from the AtoD conversion of a known noise free input voltage, the reading would fluctuate by around ±10μV in a random fashion. Clearly there is no such thing as a noise free voltage source. How much noise is attributable to the DAQ I218 and how much to the source being measured is very difficult to quantify. This means that the normal, non post-processed data from the DAQ I218 is good for about 18 BITS or less.
((input_span)/(2^{18}) ≈ 20μV where input_span is 5V)
Theoretically the AD7710 should be able to resolve to 1.7μV on this setting.

ENOB vs DATA RATE

FOR AD7710 DEVICE

BASED ON RMS NOISE



2.3 POSSIBLE SOURCES OF ERROR

The AD7710 is excellent at automatically cancelling out end-point errors. It has a built in μController to allow it to compensate for its own internal errors induced in its "perceived" GND reference and its Vref reference. This means that immediately after calibration, the AD7710 will know exactly what levels to base its AtoD conversion algorithm on. It is also possible to arrange for a "system" calibration to be performed that can also cancel end-point errors induced by the front end circuitry on the DAQ i218 card. This might necessitate some additional off-card electronics and could be controlled using the digital IO pins. The idea is to switch Vref into the converter and ask for a system slope calibration. If you have unused A inputs to the card then you could simply tie one of these to the Vref output inside the 32-way IO plug. Switch to this "spare" channel and invoke the calibration sequence. See the AD7710 data sheet for full details of how to achieve this.

The following is a list of possible error sources that should be considered:

1. The source impedance that the AD7710 "sees" must not go above 10K, otherwise errors will occur due to the way that the AD7710 takes "bursts" of charge from the source. This 10K includes the 2K of the input muxes.
2. The input leakage current for the AD7710 (10pA max.) will tend to cause DC errors due to the voltage induced across the source impedance. This can be reduced by system calibration and use of differential mode. In single ended mode, the -ve terminal of the AD7710 is switched to AGND and so does not suffer the 2K mux impedance. This will cause an imbalance.
3. Avoid ground loops in single ended mode. These can be caused when the source's -ve side is connected via the DAQ i218 cable to AGND and to the shield on the DAQ i218's connector. This shield is connected to the PC's chassis and so to "earth"(via the gold ESD strips on each side of the card). The source's -ve side (unless floating) will be the local GND and if this too is connected "earth" then if there is any difference between the two "earth" potentials current will flow in the AGND wire between the source and the DAQ i218 causing offset voltages (due to I x R losses) (the current will return through the mains wiring). Avoid

such loops by not connecting the DAQ i218 shield to any other terminal (the DAQ i218 already internally links the shield to the PC's "earth"). You may also get problems if you simply connect the shield to "earth" at the source end; again differences in local "earth" potential will cause currents to flow in the shield.

4. Avoid long connections to the DAQ i218 analogue inputs.
5. Keep AGND and DGND separate. Any digital switching currents that are allowed to share the same return path as analogue signals will result in IxR induced voltage noise. AGND and DGND are linked inside the DAQ i218 at a "star-point". All digital front-end circuits use a separate ground trace to the front-end analogue circuits to avoid such switching noise problems on the card itself. The AGND/DGND link occurs at the PCMCIA 68-way connector.
6. If your source is completely "floating" e.g. a battery, and you are using differential inputs to measure its voltage, be sure that the common mode input range of the DAQ i218 is not exceeded by connecting a medium to large (10K-100K) valued resistor between the -ve side (B input) of the source and AGND. This will provide a reference to "shift" the battery's overall potential (relative to the PC) to within the common mode range of the DAQ i218. For example, the battery could be floating several tens volts above the PC's AGND level, having been charged, say, by static electricity. Without the resistor the DAQ i218 would see the +ve battery terminal as being at $(50+V_{A1})$ and the negative as being at $(50+V_{B1})$ (assuming a 50v potential and that the + terminal links to the 'A' input on the DAQ i218 and the - terminal to the 'B' input on the DAQ i218). Fitting the resistor would "pull down" the battery's overall potential to AGND so that its "terminal" voltage can be measured.

3. DAQ i218 SOFTWARE CONSIDERATIONS

3.1 CONTROLLING THE DAQ i218

The techniques to acquire AtoD conversion results etc. follow the handshake protocol as defined in the Analogue Devices AD7710 data sheet.

3.2 CONVERTER SYNCHRONISATION

The most important point to remember about the DAQ i218 is that it is a free-running converter; that is, as soon as the previous conversion has been read out of the device, another will become available some time between 0 and t_s seconds later. The variability will only arise if there is considerable variation between the points at which the software tests the DAQ i218 for a sample to be ready. Normally this will not be the case. A conversion result will stay in the output data buffer until it is read out by software. All conversions that happen while there is a valid result waiting (if any) will be thrown away by the AD7710 (so no IRQs will be generated).

There are two methods of synchronising the software to the DAQ i218's sample outputs.

POLLING:

In a dedicated software thread that is doing nothing except acquiring sample data, the situation is very straight forward. Poll the DAQ i218 for the "sample ready flag", read the sample, continue with the polling. If channel scanning is also required then a little more thought must be applied. After changing channel, a settling time must be allowed which should be 4 x t_s for the worst case step input change (t_s is the sample period = 1/data rate). Once this period has elapsed then a dummy sample read must be performed to "waste" the conversion result that the AD7710 currently holds. Then re-poll the AD7710 until the "true" result is ready. The reason for this is that the AD7710 will not overwrite its current result until it has been read out. Assuming that the channel change moved from Chan0 to Chan1, then the conversion result that must be "wasted" will be an erroneous intermediate level between

Chan0 and Chan1. If the settling time is not obeyed, the result will be an effective "smearing" of the input channels, i.e. Chan0 will effect Chan1's apparent level, Chan1 will effect Chan2's etc. The settling time on channel selection is VERY important. Remember too that the same sample "waste" technique must be used on entry to the loop to ensure that the first conversion result is a properly settled conversion from Chan0.

The penalty of polling is that the software is effectively "idle" for nearly 100% of its time and is so very inefficient.

INTERRUPTS:

Rather than poll the converter, it is possible to set it to produce a hardware interrupt request when a new sample is ready to be collected. By writing an interrupt service routine (ISR) to handle such an event then the processor can be "freed" to do more useful tasks while the DAQ i218 generates its samples.
Two configurations will be described; i) single channel and ii) multi-channel.

i) Single channel
The ISR is configured to simply read the sample from the DAQ i218 and to clear the interrupt event in the DAQ i218 by toggling BIT5 of the SETUP register. We advise that you do not use pulse mode interrupts on PC based platforms. They are very prone to getting "lost" in the system. Instead use level mode by setting BIT6 in the CONFIG register in attribute space (see section 4). Remember to do a dummy read to clear the current sample so as to allow the converter to start making interrupts on subsequent conversions.

ii) Multi-channel
Things get more complex here, as a settling time is required after each channel change that can run into 100s of milliseconds. Clearly there is no point in waiting inside the ISR for this length of time and indeed, it will very likely crash the host if this is attempted.
The easiest solution is to make the ISR change channel and take readings but to dwell on each channel for n samples. By arranging that n x t_s is a sufficient settling period and by throwing away (n-1)

of the acquired samples, all conditions will be met. The following pseudo code fragments may help to clarify this:

INITIALISATION:

```
Set Channel0
Set Level mode IRQ
Configure DAQ I218 sample rate + gain etc.
ISR counter = 0
Initialise ISR buffer pointer
Hook ISR
Enable IRQ
Read Sample from DAQ I218 to get first IRQ
```

IRQ

ISR:

```
Read Sample from DAQ I218
ISR counter ++
Clear IRQ in DAQ I218        //ready for next sample's IRQ
If ISR counter == 5      //keep 5th sample i.e. settle time = 4 x ts
{
        Store sample at buffer pointer
        buffer pointer ++
        Channel ++        //next channel
        Set Channel
        ISR counter = 0   //ready to waste 4 samples from new chan
}
```

Remember that this will reduce the effective output data rate per channel by a factor of 5.

4. DAQ i218 REGISTER INTERFACE

The DAQ i218 decodes the incoming PCMCIA interface. It maps the CIS EPROM to 0-3FF,800-BFF etc. in attribute space. The range 400-7FF is occupied by the PCMCIA config register inside the FPGA (it repeats every byte). Both the CIS and config register are always active.

The config register is used as a master enable, as defined by PCMCIA 2.01. That is, when a valid config is written in bits0..5 the card's I/O interface may function. Until this has happened, the card's I/O interface is disabled. A **CONFIG value of 0** will disable the card (NB this is the reset state). **Valid CONFIG values are 01_d or 02_d.**

A **CONFIG value of 000001_b** will enable interrupts (if generated and secondary enabling is ON) whereas a **value of 000010_b** will disable interrupts. Bit6 of the register controls level or pulse mode nIRQ operation and bit7 acts as a soft reset when set (the reset does not clear bit7 but a subsequent write to the config register to return bit 7 to zero should not attempt to load data into bits 6..0 of the register as they will still clear. This should be done as a separate write operation.)

BIT0	Config value LSB
BIT1	.
BIT2	.
BIT3	.
BIT4	.
BIT5	Config value MSB
BIT6	Level mode nIRQ if set
BIT7	apply internal RESET when set

CONFIG Register at 400h in Attribute

All DAQ i218 functions are accessed via two I/O ports (as mapped by the host controller). The DAQ I218 only decodes A0, giving an Index register and a Data register (IR,DR). The IR is at the even

address. It is 8-bits wide and is read/write. The IR selects which internal register is to be read/written via the DR (cf 82365 PCIC). The DR is also 8-bits wide. It is the job of the host socket controller to map the IR and DR registers into the system's IO space.

The following list shows the indexes of the various registers in the DAQ i218 FPGA:

IR	DR write	DR read
0	IOPIN1..8 DATA	IOPIN1..8 i/p STATE
1	SERIALISER LOW	SERIALISER LOW
2	SERIALISER MID	SERIALISER MID
3	SERIALISER HIGH	SERIALISER HIGH
4	AUX SETUP REG	REVISION/MISC STATUS
5	BANK0 DIR	BANK0 DIR
6	CONTROL REG	CONTROL REG
7	SETUP REG	SETUP REG
8	NOT USED	READ COUNT LOW
9	NOT USED	READ COUNT HIGH

Index Allocations in the DAQ i218

NOTE

All signals with an 'n' prefix are active low in this document

4.1 IOPIN1..8 DATA/STATE REGISTERS (IDX 0)

If an IO pin is set as an output via the BANK0 DIRECTION register, then the DATA bit sent to that pin will directly control its output state. The byte sent to the DATA register for bank0 corresponds bit-for-bit with the IO pins with the LSBit of the byte controlling the lowest numbered IO pin.

Reading the STATE register will return the bit-mapped state of the bank's IO pin input latches (transparent OR frozen depending on the mode of operation).

The power on state of all IO DATA registers is 00h.

4.2 BANK0 DIRECTION (IDX 5)

This is an 8-bit register. BANK0 has resolution to allow any number of inputs and outputs within the 8 total IO pins. The structure of the register is as follows:

BIT0	DIRECTION OF BANK0 PIN1
BIT1	DIRECTION OF BANK0 PIN2
BIT2	DIRECTION OF BANK0 PINS3&4
BIT3	DIRECTION OF BANK0 PINS5,6,7&8.
BIT4	BANK0 PINS1-8 OPEN DRAIN MODE (if set as O/P).

A '1' in any bit position between bit 0 and bit 3 makes the IO pin(s) an output. The power up state is “all inputs”. Setting bit 4 enables OPEN DRAIN mode for all IOPINs configured as outputs. In this mode, the driver can sink 4mA to GND and can pull up via the PIN’s 47K pull resistor (if the pull direction is set to “up”).

4.3 AUX SETUP REGISTER (IDX 4)

This register is write only and provides a "grab-bag" of left over control bits. Its layout is as follows:

BIT0	ALWAYS LEAVE AT 0
BIT1	1=ENABLE IO PIN 2 AS CLOCK (if its an O/P)
BIT2	\ CLOCK DIVISOR CODE; 0=10MHz, 1=5MHz
BIT3	/ 2=2.5MHz, 3=1.25MHz
BIT4..7	RESERVED (KEEP AT '0')

NB: POS="POWER ON STATE" (and after a reset)

4.4 REVISION/MISC STATUS REGISTER (IDX 4)

The bottom 6 bits give the chip ID and revision code. The top two bits are used for status monitoring, as follows:

BIT0	ID CODE LSBit
BIT1	.
BIT2	ID CODE MSBit
BIT3	REV CODE LSBit
BIT4	.
BIT5	REV CODE MSBit
BIT6	nIRQSTATE
BIT7	nDRDYSTATE

The ID code will be 0. The REV code will follow the revision of the FPGA and is currently at 2.
nIRQSTATE reflects the status of the internal +ET flip flop used to turn pulsed IRQs into level IRQs. It can be set via the SETUP REG and is cleared by the rising edge of a correctly routed interrupt (i.e. activates an interrupt).

nDRDYSTATE can be used to poll when a new data word is available from the converter. It will go low when the data is ready or when a calibration sequence has completed.

4.5 SETUP REGISTER (IDX 7)

This register controls the major housekeeping functions of the DAQ I218. Its layout is as follows (NB POS="Power On State"):

BIT0 IO PIN PULL DIRECTION 1=UP (via 47K)

BIT1 CLOCK EDGE. 0=count +ve edges. Toggling this bit in S/W can be used to simulate clock edges i.e. INTERNALCLK = BIT1 xor CTCLK (NB only if the counter's gate is enabled...see BIT7)

BIT2 IRQEN POS=0. Master interrupt enable. IRQs enabled if BIT 2 is set and the CONFIG register is loaded with 01h.

BIT3 IRQSOURCE POS=0. Selects the IRQ source, between nDRDY, or from IO PIN 1 from the user interface. The interrupt on IO PIN 1 is active at the rising edge. The DAQ I218 conditions this edge to form an 800ns pulse to the PCMCIA interface if pulse mode interrupts are configured.
BIT3=1 selects IO PIN 1.

BIT4 ENLATCH POS=0. When BIT 4 goes high, input pin states are latched into internal transparent latches. This is "snapshot" mode. When BIT4 is low the latches operate in transparent mode.

BIT5 nIRQCOMPLETE POS=0. This bit connects directly to the interrupt detect flip flop's nPRESET input. Leaving it low when level mode interrupts are selected will prevent interrupts and cause the nIRQSTATE status to read back as '1'. Setting it high will release the pre-set state. A rising edge from an interrupt will cause the f/f to reset. Use this bit, set high-low-high to clear the interrupt f/f for level mode operation. This bit has no effect for pulse mode interrupts. You are advised to use level mode interrupts and use this bit to handshake that the interrupt has been serviced.

BIT6 COUNTERRESET POS=0. This is a direct reset control to the 16-bit counter timer in the DAQ I218. The counter is reset as the bit goes from 1 to 0. It must be returned to 1 to release the reset state ready for counting.

BIT7 CTGATE POS=0. This bit can be used to enable the 16-bit counter. The external GATE input is pulled down so that it can be left as "no-connect". In this state, setting BIT

7 high will allow the counter to run. If external gate control is required, this bit MUST be left reset.

4.6 SERIALISER LOW/MIDDLE/HIGH (IDX 1,2,3)

These three registers allow serial to parallel conversion for communication to the AtoD converter. They are all read/write. All clocking of the shift register is performed, under handshake control, by the AtoD. The data will be transmitted by the DAQ i218 logic with the MSB of the HIGH byte sent first. The data will be received by the DAQ i218 logic with the MSB of the 24-bit word ending in the MSB of the HIGH byte.

When transmitting a word, the serialiser "re-circulates" the data. Hence, performing a serial transmit and then reading the three registers will return the same 24-bit word back as was sent.

4.7 CONTROL REGISTER (IDX 6)

This register performs all the hand-shake functions required to "talk" to the AtoD. It also is used to set the input MUX channels etc. Its BIT layout is as follows:

BIT0 INPUT MUX ADDR BIT 0. This is the least significant bit of the 3/4 bit word which controls which input channel will be sampled.

BIT1 INPUT MUX ADDR BIT 1.

BIT2 INPUT MUX ADDR BIT 2. In DIFFERENTIAL mode this is the MSB of the input mux control word. Hence in this mode, one of eight channels can be selected. In SINGLE_ENDED mode, this bit becomes the second MSB of a 4 bit mux control word.

BIT3 INPUT MUX ADDR BIT 3. In DIFFERENTIAL mode this bit is DON'T CARE. In SINGLE_ENDED mode this bit is the MSB of a 4 bit mux control word. This gives access to one of sixteen channels.

BIT4 SINGLE_ENDED POS=0. When set this bit places the card into SINGLE_ENDED operation with 1-of-16 channels. When reset the card operates in DIFFERENTIAL mode with 1-of-8 inputs.

BIT5 nRFS. Sync handshake for logic to receive data word.

BIT6 nTFS. Sync handshake for logic to transmit data word.

BIT7 A0. Address line to AtoD.

4.8 READ COUNT LOW/HIGH (IDX 8,9)

Both ports are 8 bits wide. Reading the count value whilst the counter is running will snapshot the current count value into a temporary latch. For this to work correctly, the read sequence MUST be LOW then HIGH. After a hardware or software reset, the counter is set to FFFFh. Subsequent counter pulses will roll this over to 0000h, 0001h,0002h etc. The counter will NOT stop at FFFFh, it will roll back to 0000h. If the reset count is a problem for some applications, a dummy clock pulse can be simulated by bit manipulating the SETUP register.

The counter can run at 6MHz maximum.

5. HARDWARE SPECIFICATION

HIGHLIGHTS

- 21 BIT RESOLUTION SAMPLING A-to-D CONVERTER
- SUPERIOR NOISE REJECTION
- 8 DIFFERENTIAL / 16 SINGLE ENDED INPUT CHANNELS (SOFTWARE SELECTABLE)
- 8 DIGITAL I/O LINES (PROGRAMMABLE AS INPUT OR OUTPUT)
- 1 COUNTER/TIMER
- SOFTWARE PROGRAMMABLE SAMPLING RATES UP TO 1KHz ON A SINGLE CHANNEL (INCLUDING 50/60Hz MODE FOR LOW NOISE)
- SOFTWARE CHANNEL POLLING FOR FLEXIBILITY.
- 0-(2.5/n) V OR +/-(2.5/n)V INPUT RANGES (SOFTWARE SELECTABLE, n=1,2,4,8,16,32,64,128)
- AUTOMATIC SOFTWARE CALIBRATION FEATURE MAKES UNIT "POT-FREE"
- BACKGROUND CALIBRATION MODE FOR AUTOMATIC "HIDDEN" REMOVAL OF TEMPERATURE / DRIFT EFFECTS.
- TYPE II PCMCIA CARD FORM FACTOR WITH 32-WAY MINI D-TYPE CONNECTOR
- LOW POWER CONSUMPTION FOR PORTABLE APPLICATIONS

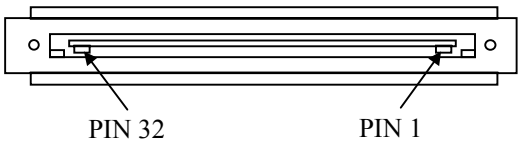
APPLICATIONS

- HIGH ACCURACY PC-CONTROLLED VOLTMETER
- CHROMATOGRAPHY
- TEMPERATURE MEASUREMENTS (THERMOCOUPLE)
- WEIGHING
- HIGH PRECISION MULTI-CHANNEL CONTROLLER AND ACQUISITION SYSTEM

FULL SPECIFICATION:

PINOUT

PIN	FUNCTION
1	ANALOGUE GROUND (0V)
2	A 0 (SINGLE ENDED CH0, DIFF CH0+)
3	B 0 (SINGLE ENDED CH8, DIFF CH0-)
4	A 1 (SINGLE ENDED CH1, DIFF CH1+)
5	B 1 (SINGLE ENDED CH9, DIFF CH1-)
6	A 2 (SINGLE ENDED CH2, DIFF CH2+)
7	B 2 (SINGLE ENDED CH10, DIFF CH2-)
8	A 3 (SINGLE ENDED CH3, DIFF CH3+)
9	B 3 (SINGLE ENDED CH11, DIFF CH3-)
10	A 4 (SINGLE ENDED CH4, DIFF CH4+)
11	B 4 (SINGLE ENDED CH12, DIFF CH4-)
12	A 5 (SINGLE ENDED CH5, DIFF CH5+)
13	B 5 (SINGLE ENDED CH13, DIFF CH5-)
14	A 6 (SINGLE ENDED CH6, DIFF CH6+)
15	B 6 (SINGLE ENDED CH14, DIFF CH6-)
16	A 7 (SINGLE ENDED CH7, DIFF CH7+)
17	B 7 (SINGLE ENDED CH15, DIFF CH7-)
18	DIGITAL GROUND (0V)
19	IOPIN 1 (with 47K prog pull up/down)
20	IOPIN 2 (with 47K prog pull up/down)
21	IOPIN 3 (with 47K prog pull up/down)
22	IOPIN 4 (with 47K prog pull up/down)
23	IOPIN 5 (with 47K prog pull up/down)
24	IOPIN 6 (with 47K prog pull up/down)
25	IOPIN 7 (with 47K prog pull up/down)
26	IOPIN 8 (with 47K prog pull up/down)
27	CTGATE (with 47K pull down)
28	CTCLK (with 47K pull down)
29	VCC (+5V) (200mA max)
30	-5V (5mA max)
31	Vref (2.500V) (1mA max)
32	Iout (20uA)



MATING CONNECTOR TYPE: HIROSE NX30TA-32PAA + NX-32TA-CV1 + NX-32T-BS

ANALOGUE:

The DAQ i218 is based around Analogue Devices' AD7710 chip. For full operating details and special functions the reader is directed to the relevant data sheets for this device.

RESOLUTION:

THE FOLLOWING DESCRIPTION REFERS TO THE AD7710 CHIP, NOT NECESSARILY TO THE DAQ i218 CARD.

21 EFFECTIVE BITS AT INPUT BANDWIDTH OF 2.62Hz AND GAIN (n) OF 1.
WORST EFFECTIVE RESOLUTION AT SAME INPUT BANDWIDTH IS 16.5 BITS WITH GAIN OF 128. FULL 21 BIT NO-MISSING-CODES PERFORMANCE. MAX SAMPLE RATE IS 1KHz (3dB BW=262Hz) (RESOLUTION REDUCES AS SAMPLE FREQUENCY INCREASES).

TYPICAL EFFECTIVE RESOLUTIONS, BITS (USING BIPOLAR INPUT MODE):

FIRST NOTCH FREQ & OUTPUT DATA RATE (Foutput)	-3dB FREQ	GAIN= 1	GAIN= 2	GAIN= 4	GAIN= 8	GAIN= 16	GAIN= 32	GAIN= 64	GAIN= 128
10Hz	2.62Hz	21.5	21.5	21	20.5	19.5	18.5	17.5	16.5
25Hz	6.55Hz	20.5	20.5	20	20	19	18	17	16
30Hz	7.86Hz	20.5	20	20	19.5	18.5	18	17	16
50Hz	13.1Hz	19	19	19	18.5	18	17.5	16.5	15.5
60Hz	15.7Hz	18.5	18.5	18.5	18.5	18	17	16.5	15.5
100Hz	26.2Hz	16.5	16.5	16.5	16.5	16.5	16.5	15.5	15
250Hz	65.5Hz	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13
500Hz	131Hz	11	11	11	11	11	11	11	11
1KHz	262Hz	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5

EFFECTIVE RESn. = (20 x LOG ((2*Vref) / (OUTPUT RMS NOISE * GAIN)) -1.76) / 6.02 (BITS)

FILTERING:

THE ON-CARD DIGITAL FILTER HAS A $\mathbf{(sinx/x)^3}$ FORM. THE NOTCHES OF THE FILTER LIE AT **(n x Foutput)** WHERE n=1,2,3...ETC. **Foutput** IS PROGRAMMED IN SOFTWARE USING A 12 BIT CODE AND IS EQUAL TO:

Foutput = 19531.25 / CODE ± 0.5% Hz (WITH CODE BETWEEN 19 AND 2000 INCLUSIVE).

THE FILTER'S ATTENUATION AT A GIVEN FREQUENCY IS:

Attenuation = –20 x LOG ([^{3}SIN (π x F / Foutput)^3 / (π x F / Foutput)]^3) dB

WHERE **F** and **Foutput** are both in Hz.

INPUT SAMPLING RATES:

THE **INPUT** SAMPLING RATES AT THE VARIOUS GAINS ARE SHOWN IN THE FOLLOWING TABLE. **DO NOT** CONFUSE THESE WITH THE ACTUAL SAMPLING RATES THAT RANGE FROM 10Hz TO 1000Hz.

NO ANTI-ALIASING IS PROVIDED ON CARD. THE INPUT DIGITAL FILTER WILL REJECT INPUT FREQUENCIES EXCEPT AT INTEGER MULTIPLES OF THE INPUT SAMPLING RATE (WITHIN A 3dB BANDWIDTH). DUE TO THE HIGH OVER-SAMPLING RATIO OF THE CONVERTER, NO ANTI-ALIASING IS NORMALLY REQUIRED. HOWEVER, IF THE INPUT SIGNAL IS SUBJECT TO NOISE CONTAMINATION WHICH FALLS WITHIN THESE STATED BANDS, A SIMPLE R-C SINGLE POLE FILTER SHOULD PROVIDE SUFFICIENT STOP-BAND ATTENUATION. IT SHOULD BE BORNE IN MIND THAT THE OUTPUT IMPEDANCE OF THE FILTER MUST NOT EXCEED THE STATED MAXIMUM LISTED UNDER THE "ANALOGUE VOLTAGE INPUTS" SECTION OF THIS SPECIFICATION.

GAIN=	INPUT SAMPLING RATE	TYPICAL INPUT IMPEDANCE
1	20KHz	2.5MΩ
2	40KHz	5.0MΩ
4	80KHz	10.0MΩ
8	160KHz	20.0MΩ
16	160KHz	20.0MΩ
32	160KHz	20.0MΩ
64	160KHz	20.0MΩ
128	160KHz	20.0MΩ

LINEARITY:

TYPICALLY ±0.0015% OF FULL SCALE.

REFERENCE:

LEVEL: 2.500V ±5mV AT 25^{O}C.
OUTPUT NOISE TYP: 8uVp-p FROM 0.1Hz TO 10Hz.
TYPICAL DRIFT: 10ppm/^{O}C (max 25). THIS DRIFT CAN BE CANCELLED DYNAMICALLY BY INVOKING A CALIBRATION SEQUENCE, OR USING BACKGROUND CAL MODE.

REFERENCE CAN BE ACCESSED EXTERNALLY.

REFERENCE LEVEL IS STORED IN CARD CIS AT MANUFACTURE TIME ACCURATE TO ± 50uV AT ROOM TEMPERATURE (THE TEMPERATURE IS ALSO STORED).

ANALOGUE VOLTAGE INPUTS:

UNIPOLAR INPUT RANGES:
0V TO i)2.5V ii)1.25V iii)0.625V iv)0.3125V v)0.15625V vi)0.078125 vii)0.039063 viii)0.019531V.

BIPOLAR INPUT RANGES:
i)+2.5V,-2.0V ii)±1.25V iii)±0.625V iv)±0.3125V v)±0.15625V vi)±0.078125 vii)±0.039063 viii)±0.019531V.

NOTE: The negative input range is limited by the input multiplexers to around -2.0V. Typically at 25^{o}C the card will pass signals down to around -2.2V but this figure is not guaranteed and is a function of the system Vcc applied to the DAQ I218 by the host controller.

ALL ANALOGUE INPUTS ARE PROTECTED TO ±35V (RELATIVE TO CARD'S GND) WITH THE CARD UNPOWERED. POWERED PROTECTION IS TYPICALLY TO ±25V.

COMMON MODE REJECTION AT DC IS AT LEAST 100dB. COMMON MODE REJECTION AT 50/60Hz IS AT LEAST 100dB (IF DATA RATE IS PROGRAMMED APPROPRIATELY).

MAXIMUM ALLOWABLE SOURCE IMPEDANCE IS TYPICALLY 8Kohms (HIGHER IMPEDANCES WILL CAUSE OFFSET ERRORS).

OTHER FEATURES:

- AMBIENT TEMPERATURE MEASUREMENT ON CARD. CAN ALLOW USER ERROR-TRAP CONDITIONS IF TEMPERATURE EXCEEDS REQUIRED LIMITS. SLOPE RATE IS +2mV/^{o}C.

- SENSOR EXCITATION CURRENT. A FIXED 20uA ±2% CURRENT, WITH 40ppm/^{o}C DRIFT (TYP). CAN BE USED FOR COLD-JUNCTION COMPENSATION ON THERMOCOUPLES. THIS CURRENT IS AVAILABLE AS “Iout” ON THE 32 WAY CONNECTOR. CONTACT INES FOR A SPECIAL VERSION OF THE DAQ I218 WHERE THIS CURRENT IS INJECTED “AHEAD” OF THE INTERNAL ANALOGUE MULTIPLEXERS.

- SENSOR BURN-OUT CURRENT. A FIXED 100nA CURRENT CAN BE DRIVEN OUT OF THE CURRENTLY SELECTED CHANNEL (ON THE A SIDE FOR DIFFERENTIAL MODE). CAN BE USED TO CHECK THAT SENSOR IS NOT OPEN CIRCUIT.

- END OF AtoD CONVERSION CYCLE CAN TRIGGER A HARDWARE INTERRUPT, FREEING APPLICATION FROM TIME CONSUMING "POLLING" OPERATIONS.

- ON CARD CALIBRATION CAN BE USED TO COMPLETELY "NULL-OUT" OFFSET AND GAIN ERRORS IN THE SYSTEM AND CONVERTER. THIS CAN BE PERFORMED ON AN "AS-REQUIRED" BASIS OR AUTOMATICALLY EVERY CONVERSION (REDUCING THE OUTPUT DATA RATE BY A FACTOR OF 6). THE LATTER FREES THE USER FROM HAVING TO WORRY ABOUT "LONG-TERM" TEMPERATURE CHANGES AND POWER-ON SETTLING EFFECTS ETC AS THEY ARE ALL CANCELLED EVERY CONVERSION. ONLY SHORT TERM DRIFTS WILL CAUSE ERRORS AND ALL ON CARD COMPONENTS HAVE BEEN CHOSEN TO ENSURE EXCELLENT "SHORT-TERM" STABILITY.

- USING THE DIGITAL I/Os AS CONTROL LINES WILL ALLOW A SCHEME WHEREBY THE CARD CAN BE CALIBRATED AGAINST A KNOWN MAXIMUM SIGNAL LEVEL RATHER THAN THE INTERNAL Vref. IN THIS WAY THE SPAN CAN BE DYNAMICALLY ALTERED TO ENSURE THAT THE MAXIMUM INPUT LEVEL WILL ALWAYS CAUSE A FULL SCALE OUTPUT CODE.

DIGITAL:

- 8 USER PROGRAMMABLE DIGITAL I/O'S. CAN BE SOFTWARE CONFIGURED TO ANY NUMBER OF INPUTS/OUTPUTS.
- OUTPUTS CAN BE SET TO OPEN-DRAIN MODE WITH A 47K PULL UP/DOWN RESISTOR ON EACH LINE (UP/DOWN DIRECTION IS GLOBAL).
- I/Os CAN SOURCE / SINK 4mA AT TTL LEVELS.
- SOFTWARE CONTROLLED INPUT LATCHES CAN BE SET TO TRANSPARENT OR ...
- ...SOFTWARE CONTROLLED "SNAP-SHOT" MODE.
- ONE DIGITAL I/O CAN BE ASSIGNED TO A USER HARDWARE INTERRUPT. ANOTHER CAN BE SET TO ACT AS A PROGRAMMABLE FREQUENCY GENERATOR OUTPUT (10MHz,5MHz,2.5MHz,1.25MHz (DUTY CYCLES NOT 50%)).
- SINGLE 16-BIT COUNTER WITH "CLK" AND "GATE" INPUTS ACCESSIBLE TO USER. SOFTWARE CONFIGURABLE ACTIVE "CLK" EDGE. SOFTWARE CONTROLLABLE "GATE". MAXIMUM COUNT FREQUENCY 6MHz. SOFTWARE RESET CONTROL. COUNTER CAN BE READ WITHOUT STOPPING COUNT.

OTHER:

- TYPE II PCMCIA CARD COMPLIANT WITH PCMCIA REL 2.1. FULL CARD INFORMATION STRUCTURE. ON CARD CALIBRATION DATA ACCESSIBLE TO USER. CIS IS "WINDOWS 95" READY.
- LOW POWER CONSUMPTION: 5V @ 20mA AVERAGE (TYP)
- 32 WAY SHIELDED I/O CONNECTOR ALLOWS CHOICE OF CABLING.
- 2-BYTE I/O INTERFACE MAKES SYSTEM INTEGRATION EASY AND SIMPLIFIES SOFTWARE CODING. ALL DATA WIDER THAN 8-BITS CAN BE READ AS 8-BIT "CHUNKS" i.e. OUTPUT FROM CONVERTER IS READ AS 3x 8-BIT BYTES).

6. OPERATIONAL PRECAUTIONS

Unless otherwise stated, all voltage levels are referenced to the DAQ i218's DIGITAL GROUND PIN.

- Don't leave active signals connected to the digital IOPINS or CTGATE, CTCLK that are capable of sourcing more than a few mA whilst the DAQ i218 itself is unpowered. This could lead to "reverse powering" the card via its inputs which can cause latch-up and destruction of internal cmos devices. If there is a possibility of this condition occurring, you are advised to connect series resistors between your drivers and the DAQ Ii18's inputs to affect current limiting (typ 4k7). Remember that this will slow the edges of the digital signals.
- Don't draw excessive current from VREF, VCC, -5v. The limits are shown in the pinout table. Doing so will adversely effect the DAQ i218's performance and could cause damage.
- Avoid connecting "analogue ground" and "digital ground" together. Inside the DAQ i218, a connection between these two is made at a single "star point" to help reduce digital ground noise coupling into the analogue sections. If you can, keep the two returns separate in a similar fashion on your equipment.
- The 32 way IO connector is quite delicate. Don't stress it unduly.
- Don't apply analogue signals to the an and bn inputs which are greater than 25v with the card powered or 35v with the card unpowered. Levels above this will damage the DAQ i218 card.
- Don't apply digital inputs to the DAQ i218 that are greater than (system Vcc + 0.5v) where "system Vcc" is the level provided on the DAQ i218's vcc output pin. Doing so will damage the DAQ i218. Likewise, don't apply levels that are less than -0.5v to the digital inputs.
- Don't short circuit any of the DAQ i218's outputs to ground or to other outputs. This will damage the DAQ i218.
- Ensure that the card's main 5v power input on the pcmcia 68 way connector does not exceed 6.0v as this will damage internal devices. This is normally not a factor that the user of a "standard" pcmcia slot needs to consider. However, under fault conditions or an embedded design this condition may need to be given some thought to avoid damaging the DAQ i218.