Hardware Manual
12 bit DAQ Cards

ines
Messtechnik
Datenverarbeitung

1. CONTROLLING THE DAQ CARD

1.1 ACQUISITION MODES

In all modes, the DAQ XXX performs its conversions in around 2.0µs (1.66µs for the DAQ i608/i616). The conversion rate is software programmable and is achieved by "spreading-out" the conversions using the PACER clock.

1.1.1 BURST MODE

This is the mode intended for transient capture or vibration analysis.

Summary:

The DAQ XXX is set up with trigger threshold and edge. The READ and WRITE POINTERS are put into a known starting state. The pre-trigger depth is configured. The system is set into RUN mode but with trigger disabled. The DAQ XXX starts taking samples. After some elapsed time, software sets ENTRIG to on to "arm" the system. The DAQ XXX will then wait until the incoming sample data meets the trigger requirements. The buffer is circular so all the time that the card is waiting for trigger samples are being stored away into SRAM. When triggered, the READ POINTER freezes. Conversions continue until the WRITE POINTER equals the READ POINTER. Then the system halts and generates an interrupt. The PC reads out the sample data from the SRAM for display / processing.

The maximum sample rate in this mode is 500KSPS (or 600KSPS for the DAQ i608/i616). This gives a buffer fill time of 32.768ms.

The slowest sample rate is 305SPS giving a buffer fill time of 53.7s.

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1.1.2 FIFO MODE

This is the mode intended for streaming data into the PC at high speed.

Summary:

The DAQ XXX takes continuous conversions in this mode. There is no triggering. As soon as software sets RUN to on, the SRAM starts to fill. The PC must empty the SRAM at a rate at least equal to the rate at which it is being filled. An interrupt can be generated at 1/4 or 1/2 full to instruct the PC to fetch the correct amount of data from the buffer. The throughput in this mode ***is PC speed dependent***. If an overrun occurs, i.e. the WRITE POINTER catches the READ POINTER up, the DAQ XXX will come out of RUN mode automatically.

With well written Assembler/C software, 500KSPS should be possible but the speed depends heavily on what happens to the data once it is in the PC i.e. displayed / written to disk etc.
The "REP INSW" PC Assembler codes are essential to get high speed.

1.1.3 SINGLE-SHOT MODE

This is the mode intended for streaming data into the PC at very low rates.

Summary:

The DAQ XXX takes single conversions in this mode. There is no triggering. As soon as software sets RUN to on, a single conversion occurs. The PC reads the sample out. The card automatically clears the RUN state ready for the PC to set the next conversion in progress. The time between conversions is totally controlled by the PC. Remember to pre-clear the READ & WRITE POINTERS (and do not try to set any pre-trigger) prior to commanding a single conversion (this ensures that the process stops immediately after one conversion rather than filling the whole SRAM buffer).

1.2 A to D OUTPUT FORMAT / GAIN SETTING

The DAQ XXX produces 2's complement 12 bit output codes when in Bipolar mode and "true binary" 12 bit codes when in Unipolar mode. Table 1.2-1 summarises the codes.

THEORETICAL INPUT LEVEL **(F.S. = FULL SCALE)**	DAQ XXX OUTPUT CODE			
	BIPOLAR		UNIPOLAR	
	BINARY	HEX	BINARY	HEX
F.S.	011111111111	7FF	111111111111	FFF
F.S. - 1LSB	011111111110	7FE	111111111110	FFE
....	....	....	....	....
0 + 2LSB	000000000010	002	000000000010	002
0 +1LSB	000000000001	001	000000000001	001
0	000000000000	000	000000000000	000
0 - 1LSB	111111111111	FFF		
0 - 2LSB	111111111110	FFE		

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....	....	....
-F.S. + 1LSB	100000000001	801
-F.S.	100000000000	800

Remember that the size of the LSB step changes depending on the input range selected and whether you are operating in Unipolar or Bipolar mode.

20 different input ranges can be achieved with the DAQ XXX. The gain is programmed using the top four bits of SETUP REG 1 (GS0..3). The following table summarises the gains and input ranges available:

GAIN	GS0..3	DAQ XXX INPUT VOLTAGE RANGE (volts)	
		BIPOLAR	UNIPOLAR
4	0h	± 0.625	0 → 1.25
2	1h	± 1.25	0 → 2.5
4/3	2h	± 1.875	0 → 3.75
1	3h	± 2.5	0 → 5.0
4/5	4h	± 3.125	0 → 6.25
2/3	5h	± 3.75	0 → 7.5
4/7	6h	± 4.375	0 → 8.75
1/2	7h	± 5.0	0 → 10.0
4/9	8h	± 5.625	
2/5	9h	± 6.25	
4/11	Ah	± 6.875	
1/3	Bh	± 7.5	
4/13	Ch	± 8.125	
2/7	Dh	± 8.75	
4/15	Eh	± 9.375	
1/4	Fh	± 10.0	

1.3 DAQ XXX BUFFER ADDRESSING

1.3.1 BUFFER DATA ORDER

The DAQ XXX always writes its A to D conversion samples into the SRAM buffer. They can be read out directly by the PC software. 2 bytes of data get written to the SRAM for every conversion "event". The buffer is organised as follows:

Pointer Address Decreasing →

7FFF	7FFE	7FFD	7FFC	7FFB	7FFA
Sample n low byte	**Sample n high byte**	**Sample n+1 low byte**	**Sample n+1 high byte**	**Sample n+2 low byte**	**etc etc...**

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The counters that control the SRAM addressing are 15-bit down counters that address bytes. When cleared they are set to 7FFFh. Each read by the PC of a byte of data decrements the READ POINTER by one. Each conversion event decrements the WRITE POINTER by two.

1.3.2 CONTROLLING THE SRAM POINTERS

The READ and WRITE pointers are 15 bits in length. They can also be programmed to be 8,9,10,11,12,13 or 14 bits long if a "shorter" buffer length is required. To achieve this, write to the CTLEN port with a 7 bit value. The bits in this byte, referred to as the BUFFLEN byte, are used to set the buffer length in the following way:

00h→8 bit
01h→9 bit
03h→10 bit
07h→11 bit
0Fh→12 bit
1Fh→13 bit
3Fh→14 bit
7Fh→15 bit

Note: The power up state of the CTLEN port is 00h

To decrement the READ POINTER by one, do a write access to the DECR port with don't care data.
To decrement the WRITE POINTER by TWO, do a write access to the DECW port with don't care data. Remember that in FIFO mode, you may get an IREQ when changing the WRITE POINTER through a half or quarter count (just as you would if the DAQ XXX passed these points whilst running at full speed...use the SELCTRD bit to block interrupts whilst manipulating the WRITE POINTER if this is a problem...see section on interrupts).

To clear all system counters to 7FFFh do the following:
1. Write access to CLRCT port with don't care data. This will clear the bottom 8-bits ONLY (it will also pre-load the MUXSEQ counter...see section on INPUT MUX CONTROL)
2. With software, remember the value of the BUFFLEN byte (note that the CTLEN port is WRITE ONLY), write to the CTLEN port with 00h, then with BUFFLEN byte. This will clear the upper 7-bits of the counters.
3. If in FIFO mode: pulse the SELCTRD bit in SETUP REG 2 to 0-1-0 to clear the possible artificial IREQ event caused by the internal counter outputs changing state.

The READ and WRITE POINTERS can be read via port 4 and 5 (low byte high byte respectively). Bit 6 of SETUP REG 2 controls whether the READ or WRITE pointer is readable: 0→READ POINTER, 1→WRITE POINTER. Do not read either pointer while the DAQ XXX is running or samples will be stored in the wrong order in SRAM. Note that this bit is dual purpose and also serves to clear IREQ events (without having to read the SRAM).

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1.3.3 PRE-TRIGGER DEPTH

Before performing a BURST acquisition the WRITE POINTER must be pre-decremented at least once by software (i.e. 2 bytes). This will give a pre-trigger depth of 1 conversion. To make the pre-trigger depth greater simply pre-decrement the WRITE POINTER extra times, each write to the DECW port will give one conversion more pre-trigger. So to set 200 conversions for the pre-trigger depth, pre-clear the pointers (1.3.2) and then write 200 times to the DECW port (don't care data).

Remember that you must control the RUN and ENTRIG bits correctly to ensure that the pre-trigger buffer actually holds valid conversion data: the DAQ XXX could trigger before conversion results have been written into the whole pre-trigger area of SRAM. The rule is to set the DAQ XXX into RUN mode but with ENTRIG off, in software wait a minimum of (t x n) seconds before enabling trigger (t is the sample period, n is the pre-trigger depth in conversions).

1.3.4 READING THE SRAM DATA

SRAM data is accessed via a single IO port at IOBASE+2. Each read by the PC will fetch data and decrement the READ POINTER. If the DAQ XXX has halted after a BURST acquisition then the READ POINTER must be "released" temporarily to read out the A to D data. This is achieved by setting SINGLE mode (Bit 7 in SETUP REG 2). Be sure to return this bit to zero before attempting to do further BURST acquisitions.
SRAM data can be read as bytes or words. If reading bytes, read two bytes to make a 16-bit value; the data is stored in the bottom 12 bits. If reading words, read 1 word to get a 16-bit value. The word wide transfer will be broken into 2 byte wide transfers automatically by the HOST PC. Pseudo word access throughput is faster than byte access throughput. The HOST PCMCIA controller should be configured with an 8-bit wide IO window running from IOBASE to IOBASE+3 (NOT +2 else word-to-byte conversions may not work correctly).

Note that the top 4 bits of the SRAM data hold the MUXSEQ count of the conversion...see section on INPUT MUX CONTROL.

1.4 TRIGGERING

1.4.1 THRESHOLD

The DAQ XXX uses an 8-bit 2's complement OR "true binary" trigger threshold value. This is compared against the top 8-bits of the 12-bits of A to D data to decide when to trigger the card. The value loaded into the threshold register MUST be appropriate to the conversion mode selected: 2's complement for Bipolar, "true binary" for Unipolar.
In C/C++ or PASCAL the threshold is calculated as a SHORT INT in the following way:

Bipolar mode:

```
TRIGBYTE = ROUND(128*(Vtrig/Vfs));  /*Vfs = full scale input voltage */
```

Unipolar mode:

```
TRIGBYTE = ROUND(256*(Vtrig/Vfs));  /*Vfs = full scale input voltage */
```


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Remember that the value loaded into the trigger threshold register varies depending on the full scale input range selected via GS0..3.

When a trigger event occurs while ENTRIG is low in SETUP REG 1, the READ POINTER is frozen but the WRITE POINTER continues to run. Once the READ and WRITE POINTER are equal (i.e. the buffer is full) the DAQ XXX halts and sets the RUN bit in SETUP REG 1. This can be polled in software to see when the card has halted. If enabled via the HOST, this will also cause an interrupt. Software can also check the TRIGGER STATUS via Bit 5 of SETUP REG 1: a 1 indicates TRIGGERED.

Triggering is only used in BURST mode.

1.4.2 TRIGGER MODES

There are various configurations of trigger on the DAQ XXX, they are summarised below:

+ET TREDGE=1 LVL=0	**-ET** TREDGE=0 LVL=0	**>** TREDGE=1 LVL=1	**<** TREDGE=0 LVL=1
TRIGGER WHEN I/P TRANSITIONS FROM BELOW Vtrig TO ABOVE Vtrig	TRIGGER WHEN I/P TRANSITIONS FROM ABOVE Vtrig TO BELOW Vtrig	TRIGGER WHENEVER I/P IS ABOVE Vtrig	TRIGGER WHENEVER I/P IS BELOW Vtrig

The modes are programmed via SETUP REG 2.
The DAQ XXX can also be trigged externally via the nTRIGGER edge connector signal. The signal is pulled up by 10K to Vcc inside the card. Pulse the line low for a minimum of one sample period to ensure the triggering is effective. This may mean external pulse stretching is required for some applications.

1.4.3 ENABLING TRIGGER

The DAQ XXX will not trigger unless Bit 1 of SETUP REG 1 is low. This allows software to “arm” the DAQ XXX only when it is appropriate to do so i.e. after some start up condition or when the user has signalled that the system should arm ready to capture an event.

1.5 OTHER FEATURES

1.5.1 SAMPLE RATE

The SAMPLE RATE is programmed via a 14-bit divider, accessed as an 8-bit register (DIVLO) and a 6-bit register (DIVHI). The clock divider runs at 5MHz. Additionally, there is an extra

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control bit that allows subtraction of a ¼ clock period from the divider. This is located in SETUP REG 1 BIT-2 and is called “nTIMING”. The purpose of this bit is to allow additional frequencies to be obtained e.g. 571.4KSPS (at the top end).

The calculation for the two data bytes is given by:

nTIMING bit SET:

```
DIVHI = (round(1/(FSample*200E-9))-2) >> 8);
DIVLO =(round(1/(FSample*200E-9))-2) & 255);
( so FSample = 1/(200E-9 * (DIVHI:DIVLO + 2)) )
```

nTIMING bit RESET:

```
DIVHI = (round(1/(FSample*200E-9))-1.75) >> 8);
DIVLO =(round(1/(FSample*200E-9))-1.75) & 255);
( so FSample = 1/(200E-9 * (DIVHI:DIVLO + 1.75))  )
```

Where FSample is in Hz.

This gives:
FSample min = 305.1Hz (count=0x3FFF)
FSample max = 250KSPS (count=0x12 nTIMING=1 DAQ i250)
500KSPS (count=0x08 nTIMING=1)
or 625KSPS (count=0x06 nTIMING=1 DAQ i608/i616 only)

For the i508/i516 and i608/i616 the input bandwidth of the card is restricted to around 250KHz to aid with anti-aliasing requirements. For the i250 it is limited to around 120KHz. If slower sample rates are used and signals greater than the Nyquist rate are present in the input signal, some form of off card low-pass filtering may be required. This filtering can be as simple as placing resistance in line with the input signal. When adding series resistance, don’t forget that you will also tend to degrade the card’s accuracy and induce offset errors due to bias currents etc

1.5.2 INPUT MUX CONTROL

There are 8 input channels to the i508/i608 and 16 to the i250/i516/i616 The channels can be used either in single ended mode i.e. number of input channels equals 8 (i508/i608) or 16 (i250/i516/i616) OR they can be set to work in true differential mode giving 4 channels (i508/i608) or 8 channels (i250/i516/i616). Refer to the pinout table for details of which channels are “differential pairs”.
The channels are multiplexed by fault protected muxes at the “front end” of the card. The muxes are controlled by a 4-bit address generated by an up counter. The MUXSEQ register controls the counting “span” of the counter. The register is 8-bits wide and is organised as 2 x 4-bit addresses. The mux counter is pre-loaded with bits0..3 of the MUXSEQ register (start address) and counts up to bits4..7 (end address). It then wraps back to the starting address again. Before starting conversions the mux counter MUST be pre-loaded with the start address from the MUXSEQ register by writing setting the SELCTRD bit in SUR2 and then writing don’t care data to the CLRCT port (remember... i) that this will undo any setup for pre-trigger that you may have made so the order of events is important ii) to set SELCTRD low again iii) that setting SELCTRD to a 1 will clear any pending interrupt). After each conversion, the mux counter is incremented by one. The MUXSEQ register does not change during conversions; it is provides permanent storage of the start and end addresses.

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The bit significance of the 4 bit counter changes depending whether the card is in single ended or differential mode. In single ended mode all four bits are used to cycle through the input channels in the order in which they are numbered i.e. A1, A2, A3 etc. In differential mode, the MSB of the counter is not used. When loading the MUXSEQ register and operating in differential mode be sure to set both bit3 and bit7 to zero (i.e. the MSBs of the start and end addresses). In differential mode the 3 bit count value is used to cycle channels in pairs i.e. A1&A5, A2&A6, A3&A7 etc.

The following examples should clarify this:

MUXSEQ REGISTER	CHANNEL SEQUENCE	
HEX	SINGLE ENDED	DIFFERENTIAL
00	A1,A1,A1,A1....	(A1- A5), (A1-A5), (A1-A5)....
55	A6,A6,A6,A6....	(A10-A14), (A10-A14), (A10-A14)....
AA	A11,A11,A11....	INVALID
FF	A16,A16,A16....	INVALID
64	A5,A6,A7,A5,A6,A7....	(A9-A13), (A10-A14), (A11-A15), (A9-A13), (A10-A14)....
1B	A12,A13,A14,A15,A16, A1,A2,A12,A13,A14,A15,A16....	INVALID
0F	A16,A1,A16,A1,A16,A1,A16....	INVALID
18	A9,A10,A11,A12,A13,A14,A15,A16,A1,A2,A9, A10,A11...	INVALID

When the DAQ XXX stores the conversion data into the SRAM it also saves the mux counter value for the conversion in the top four bits of the 16-bit data word. This provides a useful way of keeping track of which samples came from which input channel.

The MUX address changes approximately 100ns after the track and hold enters hold mode for the current conversion.
When the DAQ XXX is running at the maximum sample rate there is 1.9µs available for the MUX and analogue inputs to settle before the next conversion occurs. To keep 12-bit resolution when scanning input channels at a high rate requires some careful thought with regard to the magnitude of the difference in voltage between successive channels. Large voltage differences causes large step changes in the analog circuits which take longer to settle to ½LSB accuracy. If this situation cannot be avoided but full channel scan rate is required then be prepared to loose some accuracy in the last few bits of the 12 bit conversion result.

1.5.3 SLEEP MODE

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The DAQ XXX can be put into a low power SLEEP mode. This effectively shuts down the internal DC-DC converters, oscillator and AtoD converter. The analogue part of the card will not function in this mode. When enabling the card i.e. coming out of SLEEP mode, allow at least 2 seconds for the power to stabilise before taking any measurements.
The card powers up in SLEEP mode and enters SLEEP mode after a hard or soft reset. Bit 3 of SETUP REG 1 controls the SLEEP state: 1→POWER ON, 0→GO TO SLEEP.

Important:
Note that after powering up the card and bringing the card out of sleep, the RUN state should be set to active then back to inactive. This allows internal clock generation to stabilise prior to taking any ADC readings. Failure to do this can show as a "bad" first sample from the ADC directly after power-up.

1.5.4 INTERRUPTS

The DAQ XXX can generate interrupts if the HOST enables the PC-Card IREQ signal to a PC interrupt channel. Using interrupts is a convenient and efficient means of keeping track of what the card is doing. Interrupts work differently depending on which mode the card is in:

MODE	CAUSE
BURST	WHEN CARD HALTS AFTER THE BUFFER HAS FILLED
FIFO	PROGRESS AS BUFFER FILLS. USE SETUP REG 2 BITS 0 AND 1 TO SELECT: 0-INTERRUPT ONLY WHEN BUFFER FULL (NO USE FOR CONTINUOUS DATA STREAMING), 1-INTERRUPT EVERY TIME THE BUFFER IS HALF FULL, 2-INTERRUPT EVERY TIME THE BUFFER IS QUARTER FULL, 3-INTERRUPT EVERY CONVERSION.
SINGLE	IGNORE ANY INTERRUPTS THAT MAY OCCUR IN THIS MODE

To actually use interrupts the HOST controller will have to be configured to route the IREQ signal to one of the PC's interrupt channels.
Note that all conditions that cause an interrupt can also be polled for in software; that is, you do not have to use interrupts. This is because the state of the internal Flip-Flop that latches the interrupt state can be read via IODIR REGISTER Bit 4: 0→INTERRUPT PENDING, 1→NO INTERRUPT.

The interrupt from the DAQ XXX is latched. It must be cleared before another interrupt can be generated. To clear it read from the SRAM buffer. It can also be cleared by a soft or hard reset or by pulsing the SELCTRD bit in SETUP REG 2 low-high-low. Note that leaving the SELCTRD bit high will block ALL IREQ events AND will stop the MUXSEQ counter from counting (this signal is used as the control to pre-load the MUXSEQ counter from the MUXSEQ register). Using the CLRCT port to reset the internal counters may cause an artificial IREQ event when in FIFO mode. Use the SELCTRD bit to clear this.

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1.5.5 CONFIG OPTION REGISTER

The DAQ XXX uses the Config Option Register or COR to enable a particular mode. The COR is at 400h in attribute space and is 8-bits wide read/write. It is organised as follows:

BIT0	Config value LSB
BIT1	.
BIT2	.
BIT3	.
BIT4	.
BIT5	Config value MSB
BIT6	Not used
BIT7	Apply internal RESET when set

The config values (6 bit) are as follows:

COR Config value	MODE
0	DISABLE CARD
1	BURST
5	FIFO

1.5.6 DIGITAL IO

There are 8 digital IO lines which can be used for general control / monitoring.
The bottom 4 bits of the IODIR register are used to configure the IOPINs as inputs or outputs. The grouping is as follows:

BIT0	DIRECTION OF IOPIN1
BIT1	DIRECTION OF IOPIN2
BIT2	DIRECTION OF IOPIN3&4
BIT3	DIRECTION OF IOPIN5,6,7&8.

Setting a bit high enables the pin/group of pins as outputs. The data to / from the pins is read via the IODATA register as an 8-bit byte and logically the bit position in the byte corresponds to the particular IOPIN that is addressed i.e. Bit 4 ⇔ IOPIN4.

Please read the section on Operational Precautions for tips on how to protect the digital IO pins if they are to be subjected to active power while the DAQ XXX itself is unpowered.

1.6 DAC PROGRAMMING

The DACs on the MF series are loaded serially using the upper four digital I/O lines (which are no longer accessible on the MF series).

The following code fragment shows how to set DAC codes up:

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```
void EXPORTFUNCTION DLL_SetDtoACodes(unsigned char skt,unsigned short code1, unsigned short
code2)
{                                   //pass in either code as 0xFFFF to load previous DAC code

   unsigned char d,dout,bit,cmds[100],cmdct=0;

   //Note: if there are two threads altering the DIO pins at the same time and this routine
   //is interrupted by the other and alters the state of the bottom 4 DIOs then this routine
   //will revert them back to their states as read by the following line of code...

         d = DLL_ReadIOPins(skt) & (unsigned char)0x0f;   //leave lower 4 DIOs alone

   //A semaphore scheme to interlock accesses could be added if this is a problem.

   if (code1 == 0xffff)
     code1 = DtoACode[0][skt];   //use last code if ffff passed in
   if (code2 == 0xffff)
     code2 = DtoACode[1][skt];

   DtoACode[0][skt] = code1;  //record the state for DtoA1
   DtoACode[1][skt] = code2;  //record the state for DtoA2

   code1 <<= 1;   //require 3 bit opcode + 12 bit data + 1 stop bit so move data + opcode one place left
   code2 <<= 1;   //to make the stop bit

   //For speed this routine "compiles" a list of byte wide Digital IO data and blats its in
   //one go using a block write.

   cmds[cmdct++] = d;  //set nCS low

   for(bit=0;bit<16;bit++)
   {
     cmds[cmdct++] = dout = d | (unsigned char)((code1 & (unsigned short)0x8000) >> 11) | (unsigned
char)((code2 & (unsigned short)0x8000) >> 10);
     cmds[cmdct++] = dout | (unsigned char)0x40;  //set clk high
     code1 <<= 1;  //next bits, NB msbit goes out first
     code2 <<= 1;
   }
   cmds[cmdct++] = dout;  //set clk low after last bit

   if (DtoAWFGMode[skt] == INACTIVE)
     cmds[cmdct++] = dout | (unsigned char)0x80;  //set nCS high to update DACs, or leave it
                                          //low so that pacer can
                                        //return it high automatically when in WFG
//mode
  ByteWriteIOPort(io_win[skt],IODATA);              //send the index for the digital IO data
  BlockWriteIOPort((unsigned short)(io_win[skt]+1),1,cmds,cmdct);  //then blat the data bytes
                                                    //in a burst
}
```

One extra feature for the two DACs is their ability to be updated in synchronism with an ADC event. After shifting in the DAC codes it is usual to return the “nCS” line to the DACs high to affect the update (the line is common to both). However, if this line is left low and “waveform generation mode” is selected the “nCS” line will be returned high automatically the next time the ADC section of the card generates an interrupt. This can be used to “pace” the DAC updates at a

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low rate. Due to the high overhead involved with loading DAC codes, DAC update rates of a few Hz can be realised.

By setting the interrupt configuration of the FIFO run mode of the card this interrupt can occur i) every sample ii) every quarter buffer (i.e. every 4096/Fsample seconds) iii) every half buffer (i.e. every 8192/Fsample seconds). Remember that the FIFO still needs to be emptied correctly for this to keep running even if you are only interested in updating DACs (otherwise the FIFO will overflow).

2. DAQ XXX REGISTER INTERFACE

The DAQ XXX decodes the incoming PCMCIA interface. It maps the CIS EPROM to 0-3FF,800-BFF etc. in attribute space. The range 400-7FF is occupied by the PCMCIA config option register inside the DAQ XXX (it repeats every byte). Both the CIS and COR are always active.

The COR is used as a master enable, as defined by PCMCIA 2.01. That is, when a valid config is written in bits0..5 the card's I/O interface may function. Until this has happened, the card's I/O interface is disabled. A config value of 0 will disable the card (NB this is the state after a reset). Valid CONFIG values are 01_d or 02_d or 05_d. See the section on the COR for details of the various modes.

Bit7 of the COR acts as a soft reset when set (the reset does not clear bit7 but a subsequent write to the config register to return bit 7 to zero should not attempt to load data into bits 6..0 of the register as they will still clear. This should be done as a separate write operation.)

All DAQ XXX functions are accessed via three I/O ports (starting at IOBASE as mapped by the host controller). The DAQ XXX decodes A0 and A1, giving an Index Register (IR) at IOBASE+0, a Data Register (DR) at IOBASE+1 and the SRAM data port at IOBASE+2&3. The IR is 8-bits wide and is write only. The IR selects which internal register is to be read/written via the DR (cf 82365 PCIC). The DR is also 8-bits wide. It is the job of the host socket controller to map the IR, DR and SRAM data registers into the system's IO space starting at IOBASE and ending at IOBASE+3.

The following table shows the indexes of the various registers in the DAQ XXX (all are 8-bits unless stated):

IR	DR write	DR read
0	SETUP REG 1 (8-BIT)	SETUP REG 1 (8-BIT)
1	SETUP REG 2	SETUP REG 2
2	IODATA	IODATA
3	IODIR (4-BIT)	IODIR(6-BIT)
4	DIVLO	ADDRCTLO
5	DIVHI (6-BIT)	ADDRCTHI
6	MUXSEQ	N/U

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7	TRIGTHRESH	N/U
8	N/U	SETUP REG 1 (8-BIT)
9	CTLEN	SETUP REG 2
A	N/U	IODATA
B	N/U	IODIR(6-BIT)
C	N/U	ADDRCTLO
D	DECR	ADDRCTHI
E	DECW	N/U
F	CLRCT	N/U

Port Index Allocations in the DAQ XXX

NOTE

1. All signals with an 'n' prefix are active low in this document.
2. All BINARY values are shown with MSBit LEFTMOST.

2.0 SETUP REG 1 (IR 0)

BIT	FUNCTION		RESET STATE
	WRITE	**READ**	
0	**nRUN** **Set low to start the DAQ XXX taking conversions or to start a SINGLE conversion.**	**nRUN**	**1**
1	**nENTRIG** **Set low to enable triggering i.e. ARM the DAQ XXX (BURST mode only).**	**nENTRIG**	**1**
2	**nTIMING** **Set low to enable a ¼ clock period subtraction from the PACER divider.**	**nTIMING**	**1**
3	**nSLEEP** **Set low to put DAQ XXX into low power SLEEP mode.**	**nSLEEP**	**0**
4	**GS0** **LSB of gain set code**	**GS0**	**0**
5	**GS1**	**GS1**	**0**
6	**GS2**	**GS2**	**0**
7	**GS3** **MSB of gain set code**	**GS3**	**0**

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2.1 SETUP REG 2 (IR 1)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	IBITSEL0 See IBITSEL1.	IBITSEL0	0
1	IBITSEL1 MSBit of 2-bit interrupt select: 00: Interrupt when buffer full 01: Interrupt every ½ buffer full 10: Interrupt every ¼ buffer full 11: Interrupt every conversion Only applies in FIFO mode.	IBITSEL1	0
2	BIPOLAR Set high to use Bipolar input ranges, set low for Unipolar	BIPOLAR	0
3	SINGLEEND Set high to use Single Ended input channels, set low for Differential	SINGLEEND	0
4	TREDGE Selects +ET when set high in non-level mode or > when set high in level mode. Selects -ET when set low in non-level mode or < when set low in level mode.	TREDGE	0
5	LVL Select level mode when set.	LVL	0
6	SELCTRD Set low to read READ POINTER or high to read WRITE POINTER. Also used to clear IREQs when set high. Set 0-1-0 to clear an IREQ. Also used to pre-load the MUXSEQ counter when high...see Input Mux Control section for details.	SELCTRD	0
7	SINGLE Set high when in FIFO mode to allow nRUN to invoke a single conversion. Set high	SINGLE	0

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	in BURST mode to “release” READ POINTER after DAQ XXX has halted to allow SRAM to be read out.		

2.2 IODATA (IR 2)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	IOPIN0 Control IOPIN0	IOPIN0 Status of IOPIN0	0
1	IOPIN1 Control IOPIN1	IOPIN1 Status of IOPIN1	0
2	IOPIN2 Control IOPIN2	IOPIN2 Status of IOPIN2	0
3	IOPIN3 Control IOPIN3	IOPIN3 Status of IOPIN3	0
4	IOPIN4 Control IOPIN4	IOPIN4 Status of IOPIN4	0
5	IOPIN5 Control IOPIN5	IOPIN5 Status of IOPIN5	0
6	IOPIN6 Control IOPIN6	IOPIN6 Status of IOPIN6	0
7	IOPIN7 Control IOPIN7	IOPIN7 Status of IOPIN7	0

2.3 IODIR (IR 3)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	IOPIN0DIR Set high to enable as OUTPUT	IOPIN0DIR	0
1	IOPIN1DIR Set high to enable as OUTPUT	IOPIN1DIR	0
2	IOPIN2&3DIR Set high to enable as OUTPUTS	IOPIN2&3DIR	0
3	IOPIN4,5,6,7DIR Set high to enable as OUTPUTS. On MF series the	IOPIN4,5,6,7DIR or WFGEN	0

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	upper four IOs are always outputs and this bit changes function to become WFGEN which enables DAC waveform generation mode when high.		
4		nIREQ Low when an interrupt request is pending.	0
5		TRIGGERED High when DAQ XXX has detected a trigger event whilst running and ARMed.	
6			
7			

2.4 DIVLO / ADDRCTLO (IR 4)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	DIV0	ADDRCT0	-
1	DIV1	ADDRCT1	-
2	DIV2	ADDRCT2	-
3	DIV3	ADDRCT3	-
4	DIV4	ADDRCT4	-
5	DIV5	ADDRCT5	-
6	DIV6	ADDRCT6	-
7	DIV7	ADDRCT7	-
	LOW 8-BIT WORD OF 14-BIT CLOCK DIVIDER. SEE ALSO THE "TIMING" BIT IN SETUP REG 1.	LOW 8-BIT WORD OF 16-BIT READ OR WRITE POINTER.	

2.5 DIVHI / ADDRCTHI (IR 5)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	DIV8	ADDRCT8	-
1	DIV9	ADDRCT9	-
2	DIV10	ADDRCT10	-
3	DIV11	ADDRCT11	-
4	DIV12	ADDRCT12	-
5	DIV13	ADDRCT13	-

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6		ADDRCT14	-
7		ADDRCT15	-
	HIGH 6-BIT WORD OF 14-BIT CLOCK DIVIDER. SEE ALSO THE "TIMING" BIT IN SETUP REG 1.	HIGH 8-BIT WORD OF 16-BIT READ OR WRITE POINTER.	

2.6 MUXSEQ (IR 6)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	MUXSEQ0 (start address LSB)		0
1	MUXSEQ1		0
2	MUXSEQ2		0
3	MUXSEQ3 (start address MSB)		0
4	MUXSEQ4 (end address LSB)		0
5	MUXSEQ5		0
6	MUXSEQ6		0
7	MUXSEQ7 (end address MSB)		0
	8-BIT VALUE USED TO CONTROL INPUT MUX SEQUENCING.		

2.7 TRIGTHRESH (IR 7)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	TRIGTHRESH0		0
1	TRIGTHRESH1		0
2	TRIGTHRESH2		0
3	TRIGTHRESH3		0
4	TRIGTHRESH4		0
5	TRIGTHRESH5		0
6	TRIGTHRESH6		0
7	TRIGTHRESH7		0
	8-BIT TRIGGER THRESHOLD VALUE.		

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2.8 CTLEN (IR 9)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	CTLEN0		0
1	CTLEN1		0
2	CTLEN2		0
3	CTLEN3		0
4	CTLEN4		0
5	CTLEN5		0
6	CTLEN6		0
7			0
	7-BIT VALUE TO CONTROL ACTIVE LENGTH OF READ AND WRITE POINTERS. ALSO USED TO FORCE A PARTIAL RESET OF BOTH READ AND WRITE POINTERS. BIT-MAPPED: 0x7F SETS 15-BIT, 0x3F-14, 0x1F-13, 0x0F-12, 0x07-11, 0x03-10, 0x01-9, 0x00-8-BIT. MUST BE 15-BIT FOR FIFO MODE.		

2.9 DECR (IR D)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	X	X	-
1	X	X	-
2	X	X	-
3	X	X	-
4	X	X	-
5	X	X	-
6	X	X	-
7	X	X	-
	ANY READ OR WRITE ACCESS TO THIS PORT WILL DECREMENT THE READ POINTER BY ONE.		

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2.10 DECW (IR E)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	X	X	-
1	X	X	-
2	X	X	-
3	X	X	-
4	X	X	-
5	X	X	-
6	X	X	-
7	X	X	-
	ANY READ OR WRITE ACCESS TO THIS PORT WILL DECREMENT THE WRITE POINTER BY TWO.		

2.11 CLRCT (IR F)

BIT	FUNCTION		RESET STATE
	WRITE	READ	
0	X	X	-
1	X	X	-
2	X	X	-
3	X	X	-
4	X	X	-
5	X	X	-
6	X	X	-
7	X	X	-
	ANY READ OR WRITE ACCESS TO THIS PORT WILL SET THE READ & WRITE POINTERS TO 0x7FFF AND WILL PRE_LOAD THE MUX COUNTER WITH THE MUXSEQ START ADDRESS. NB: CLEARING THE COUNTERS IN FIFO MODE MAY CAUSE AN ARTIFICIAL IREQ EVENT. USE THE SELCTRD BIT TO CLEAR THE IREQ FLIP-FLOP AFTER CLEARING THE COUNTERS.		

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